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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/509,478	09/29/2004	Marten Erik Van Dijk	NL 020269	1367

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EXAMINER	
CHAUDRY, MUJTABA M	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 07/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/509,478	VAN DIJK ET AL.	
	Examiner	Art Unit	
	Mujtaba K. Chaudry	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8-16* is/are rejected.

7)☒ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicants' response was received April 10, 2006.

- Claims 1-16 remain pending.
- Drawing corrections are accepted. Formal copy is needed for Figure 1.
- Abstract is accepted.
- Specification is not accepted. See reasons below.
- Rejections under 35 USC 112 are maintained and introduced by amendments.

Application pending.

Response to Amendment

Applicant's arguments/amendments with respect to amended claims 1-16 filed April 10, 2006 have been received. All arguments have been fully considered but are not persuasive. The Examiner would like to point out that this action is made final (See MPEP 706.07a).

Applicants contend, "...subheadings in the specification are not required in accordance with MPEP 608.01(a)..." The Examiner respectfully disagrees. MPEP 608.01(a) is quoted below and highlighted as appropriate.

608.01(a) [R-3] Arrangement of Application

37 CFR 1.77. Arrangement of application elements.
(a) The elements of the application, if applicable, should appear in the following order:
(1) Utility application transmittal form.
(2) Fee transmittal form.
(3) Application data sheet (see § 1.76).
(4) Specification.
(5) Drawings.
(6) Executed oath or declaration.

(b) **> The specification should include the following sections in order:
(1) Title of the invention, which may be accompanied by an introductory portion stating the name, citizenship, and residence of the applicant (unless included in the application data sheet).
(2) Cross-reference to related applications (unless included in the application data sheet).
(3) Statement regarding federally sponsored research or development.
(4) The names of the parties to a joint research agreement.
(5) Reference to a "Sequence Listing," a table, or a computer program listing appendix submitted on a compact disc and an incorporation-by-reference of the material on the compact disc
(see § 1.52(e)(5)). The total number of compact discs including duplicates and the files on each compact disc shall be specified.
(6) Background of the invention.
(7) Brief summary of the invention.
(8) Brief description of the several views of the drawing.
(9) Detailed description of the invention.
(10) A claim or claims.
(11) Abstract of the disclosure.
(12) " Sequence Listing, " if on paper (see § § 1.821 through 1.825).
(c) The **text of the specification sections defined in paragraphs (b)(1) through (b)(12) of this section, if applicable, should be preceded by a section heading in uppercase and without underlining or bold type.**<

Applicants contend prior arts of record do not teach, "...reducing the length of each row of said code block by adding x row symbols together to form y row symbols replacing the x row symbols, y being less than x, to form shortened rows according to a predetermined adding rule resulting in a reduced code block..." The Examiner respectfully disagrees and would like to point out that this argument is based on an amendment which is not clear and is addressed in 35 USC 112 section of this action. See below.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- The claim recites, **"...reducing the length of each row of said code block by adding x row symbols together to form y row symbols replacing the x row symbols, y being less than x, to form shortened rows according to a predetermined adding rule resulting in a reduced code block..."** which is not clear. For example, suppose each row of the code block has 10 symbols and we pick x (let x = 4, i.e.), then adding the 4 symbols together to form y row symbols, which is still 4 symbols. Then how is y defined to be less than x. What is y? Furthermore, adding a plurality of symbols together will not be less than the initial group—hence y can not be less x—it should maybe be greater. The claim language is vague and indefinite and perhaps missing essential elements.
- The claim recites, "...reducing the length of each row...by adding row symbols together..." The Examiner is not sure what the applicants intend to convey. For example, if Row 1 = (1 1 1 1) and Row 2 = (1 0 1 0); then adding Row 1 + Row 2 = (0 1 0 1), which is the same length. It is possible that the Examiner is misinterpreting the claim language. However, it is more likely that the claim language is missing essential elements or is inherently flawed. In any case, clarification is needed to the claims. The Examiner reserves the right to disregard this limitation while examining the claim on the merits.

Appropriate correction is required.

The Examiner disagrees with the Applicant and maintains rejections with respect to amended claims 1-16. All arguments have been considered. It is the Examiner's conclusion that amended claims 1-16, as presented, are not patentably distinct or non-obvious over the prior art of record. See office action:

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-6 and 8-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kondo (USPN 6581178) further in view of Kimura et al. (USPN 5757825).

As per claim 1, Kondo substantially teaches (abstract) an error correction coding method comprising **segmenting continuous transmission data in units of predetermined lengths,** rearranging the data in parallel, and **performing error correction coding processing for each of horizontal line blocks** and vertical line blocks of the rearranged transmission data. The Examiner would like to point out that segmenting data units into predetermined lengths is analogous to reducing the length of each row of the present application.

Kondo does not explicitly teach to embed horizontal parities within the shortened row code words as stated in the present application.

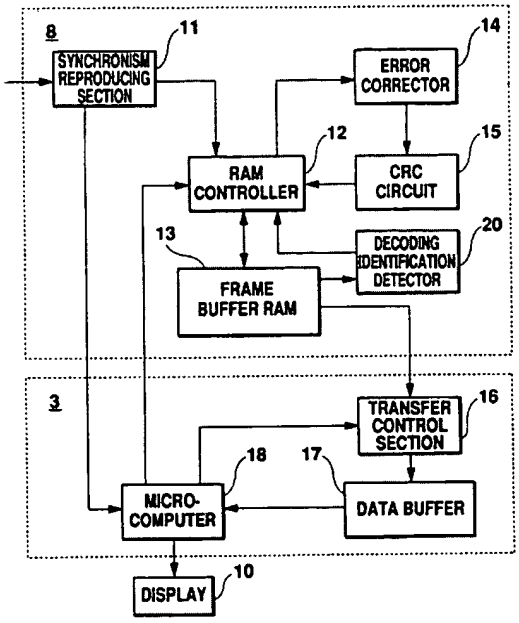

Fig. 7

However, Kimura et al. (herein after referred to as single entity: Kimura) in an analogous art, substantially teaches (Figure 7) a digital signal is composed of a frame which consists of a predetermined number of blocks in the vertical direction, a block consisting of a predetermined number of bits in the horizontal direction and having a horizontal parity (error correcting code) for correcting error in the horizontal direction and a vertical parity for correcting errors in the vertical direction. The block also has a control bit for determining whether the error correction in the horizontal direction is to be carried out only once. A decoding identification detector (20) detects the content of the control bit, a controller (12) controls the re-writing of the digital signal into a frame buffer (13) after the error correction of the digital signal in the vertical direction by an error corrector (14). The controller (12) also controls the provision of the digital signal stored in the buffer (13) to the error corrector (14) according to the content of the control bit, determining whether the second error correction in the horizontal direction is to be carried out.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to embed horizontal parities within the shortened row code words within the method and apparatus of Kondo. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill would have recognized that by embedding horizontal parities within the shortened row code words would have increased the error detection and correction capability.

As per claim 2, Kondo substantially teaches, in view of above rejections, (col. 1, lines 5-16 and elsewhere) Reed-Solomon coding. The Examiner would like to point out that Reed-Solomon coding is well-known in the art for deep-space communications which use Long Distance Codes, for example.

As per claim 3, Kondo substantially teaches, in view of above rejections, (abstract) a error correction coding method comprising segmenting continuous transmission data in units of predetermined lengths, which is analogous to reducing the length of each code word. Kondo then rearranges the data in parallel and performs error correction coding processing for each of horizontal line blocks, which is analogous to extending each row by encoding.

As per claim 4, Kondo substantially teaches, in view of above rejections, (col. 1) an error correction coding/decoding method and device and error correction decoding device using error correction using a block code. In this case, a punctured code is used at a coding rate higher than that of an original code, and high system compatibility is obtained. Although this is taught in the background section, it is well-known in the art to utilize puncturing codes, especially when performing rate matching which is necessary in LDC.

As per claims 5-6, Kondo substantially teaches, in view of above rejections, (Figure 2B) the horizontal line block error correction decoding circuit 121 and vertical line block error correction decoding circuit 122 of the error correction decoder 120 on the receiving side rearrange reception data in parallel in the horizontal direction, as on the transmitting side. Next, "0" is substituted into a variable i representing the error correction decoding processing execution count (step 211), and "1" is added to the variable i to perform decoding processing (step 212). More specifically, error correction of horizontal line blocks is performed sequentially from horizontal line 0 to horizontal line n/m-1 (step 213), and error correction of vertical line blocks is performed sequentially from vertical line 0 to vertical line m-1 (step 214). Steps 212 to 214 are repeated until the variable i reaches a predetermined processing count I (step 215).

As per claim 8, Kondo substantially teaches, in view of above rejections, (abstract) the error correction coding processing is performed for each of horizontal line blocks and vertical line blocks of the rearranged transmission data. The Examiner would like to point out that product codes are usually in matrix form, i.e. rows and columns.

As per claim 9, Kondo substantially teaches, in view of above rejections, (col. 1) the data transmission by a digital communication system or data storage by a digital storage device, error correction coding and decoding are performed to detect a data error from an error-correcting code (also called a redundant code) and correct the error to improve the reliability. As the error-correcting code, a multidimensional code such as a Hamming code, BCH (Bose-Chaudhuri-Hocquenghem) code, or Reed-Solomon code is known. The multidimensional code is originally has a plurality of bits, and allows correct burst error correction or byte error correction.

As per claims 10-11 and 13, Kondo substantially teaches, in view of above rejections, (Figures 19A-B) a Reed-Solomon code enables error correction and loss correction by adding a check symbol to an information symbol. Error correction is processing of reconstructing a correct signal transmitted by the transmitting side when symbols having errors in a received signal are unknown. Loss correction is processing of reconstructing a correct signal transmitted by the transmitting side when symbols having errors in a received signal are known. As is generally known, with the error correction ability, when 2N (N: arbitrary natural number) check symbols are present, N error symbols can be corrected. This error correction can be performed when error symbol position information (information representing a symbol having an error in a received signal) is not present. With the loss correction ability, when 2N check symbols are present, 2N lost symbols can be corrected. This correction can be performed when error symbol position information is present. The Examiner would like to point out that decoding is performed similar to that of encoding in a reverse manner.

As per claim 12, Kondo substantially teaches (abstract) an error correction coding method comprising segmenting continuous transmission data in units of predetermined lengths, rearranging the data in parallel, and performing error correction coding processing for each of horizontal line blocks and vertical line blocks of the rearranged transmission data. The Examiner would like to point out that segmenting data units into predetermined lengths is analogous to reducing the length of each row of the present application.

Kondo does not explicitly teach to embed horizontal parities within the shortened row code words as stated in the present application.

However, Kimura et al. (herein after referred to as single entity: Kimura) in an analogous art, substantially teaches (Figure 7) a digital signal is composed of a frame which consists of a predetermined number of blocks in the vertical direction, a block consisting of a predetermined number of bits in the horizontal direction and having a horizontal parity (error correcting code) for correcting error in the horizontal direction and a vertical parity for correcting errors in the vertical direction. The block also has a control bit for determining whether the error correction in the horizontal direction is to be carried out only once. A decoding identification detector (20) detects the content of the control bit, a controller (12) controls the re-writing of the digital signal into a frame buffer (13) after the error correction of the digital signal in the vertical direction by an error corrector (14). The controller (12) also controls the provision of the digital signal stored in the buffer (13) to the error corrector (14) according to the content of the control bit, determining whether the second error correction in the horizontal direction is to be carried out. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to embed horizontal parities within the shortened row code words within the method and apparatus of Kondo. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill would have recognized that by embedding horizontal parities within the shortened row code words would have increased the error detection and correction capability.

As per claims 14-16, Kondo substantially teaches, in view of above rejections, (col. 1) the data transmission by a digital communication system or data storage by a digital storage device, error correction coding and decoding are performed to detect a data error from an error-correcting code (also called a redundant code) and correct the error to improve the reliability. As

the error-correcting code, a multidimensional code such as a Hamming code, BCH (Bose-Chaudhuri-Hocquenghem) code, or Reed-Solomon code is known. The multidimensional code is originally has a plurality of bits, and allows correct burst error correction or byte error correction.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 571-272-3817. The examiner may normally be reached Mon – Thur 6:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 571-272-3819.

Mujtaba Chaudry
Art Unit 2133
June 26, 2006

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SUPERVISORY PATENT EXAMINER
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